BrainChip’s ultra-low power licensable AI IP is ideal for cost and size sensitive applications.

**KEY FEATURES**
- Complete configurable neural network processor
- Complete software development flow
- On-chip mesh network interconnect
- Standard AXI 4.0 interface for on-chip communication
- Scalable nodes can be configured as event domain:
  - Convolution neural processor
  - Fully connected neural processor
- No CPU required
- External memory optional
- Configurable amounts of embedded memory and input buffers
- Integrated DMA and data-to-event converter
- Hardware support for on-chip learning
- Hardware support for 1, 2 or 4-bit hybrid quantized weights and activations to reduce power and minimize memory footprint
- Fully synthesizable RTL
- IP deliverables package with standard EDA tools
  - Complete testbench with simulation results
  - RTL synthesis scripts and timing constraints
  - Customized IP package targeted for your application

**SCALABLE SOLUTION**
- Customer configurable for size, power, speed
- Programmable clock speed
  - Up to 300MHz in 28nm
- Parallel hardware processing
- Run-time configuration manager
  - Maps neural network to the number of nodes available

**SCALE NODES FOR YOUR APPLICATION**

One Step Solution: Layers processed in parallel

Multi-Step Solution: Layers processed sequentially

**EDGE LEARNING**
- Add new classifiers to your DNN on chip
- No need for retraining cycle
- 1-shot and multiple-shot learning
- Personalize your Edge solution

**AKIDA IP ARCHITECTURE**
AKIDA IP FOR EDGE AI

Infer and Learn at the edge with Akida’s fully customizable event-based AI neural processor. Akida’s parameterized architecture and small footprint boosts efficiency by orders of magnitude, scales to 1024 nodes connected over a mesh network. Each Node consists of 4 Neural Processing Units (NPU), each with scalable and configurable SRAM. Within each node, the NPUs can be configured as either convolutional or fully connected.

NODE FEATURES
- 4 NPUs per node
- Convolutional NPUs support
  - 160K input events, Max 512 Filters, Max 1K input Channels
  - Depthwise separable convolution or standard Convolution
- Fully Connected NPUs support
  - 160K input events 4.5K local neuron with on chip weight or 64K local neuron with external weight

IMAGE OR DATA TO EVENT CONVERTER (8BIT CONVOLUTION)
- Video input format: RGB 888 or 8-bit Grayscale
- Kernel Sizes: Strides 1, 2, 3
  - 3x3: 192 filters
  - 5x5: 64 filters
  - 7x7: 32 filters
- Max Pooling: 2x2
- Weights are 8-bit signed

AKIDA DEVELOPMENT ENVIRONMENT

AKIDA DESIGN SPACE

The Akida Neural Processing IP is highly scalable and flexible. The chart above shows a variety of solutions and the relationship between number of parameters, MACs/inference and power for 30 FPS throughput.

The Akida™ Development Environment (ADE) works with TensorFlow, Keras and other frameworks to provide developers with a complete machine learning environment designed to create, train and test Neural Networks. Once developed, quantized and trained, network models are converted to run on the Akida event domain processor simulator for full performance evaluation. ADE leverages Python alongside all associated tools and libraries – Jupyter Notebook and NumPy. ADE is comprised of the Akida Chip Simulator, data converters and a “model zoo” to integrate customers’ existing Neural Network models.